Application No.: 10/779,904 Docket No.: 02008/071003

AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. - 3. (Canceled)

4. (Currently Amended) A fault analysis method [[for]] of presuming a fault location of a semiconductor IC comprising:

applying a power supply voltage to said semiconductor IC;

- supplying a test pattern sequence having a plurality of test patterns to said semiconductor IC;
- storing a fault location list for the test pattern sequence, wherein the fault location list includes one or more locations of components in said IC, and the electric potentials at the one or more locations are expected to change [[when]] once the test pattern sequence is supplied;
- measuring <u>a time integral of</u> a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern and determining whether said transient current shows abnormality or not; and
- presuming a fault location out of said fault location list, based on said test pattern sequence, where the transient power supply current shows abnormality, and said fault location list,
- wherein said transient power supply current is determined to be abnormal in <u>a</u> case <u>that</u> <u>the</u> time integral of said transient power supply current is over a predetermined value in said step of determining.

5. - 15. (Canceled)

- 16. (Currently Amended) A fault analysis apparatus for presuming configured to presume a fault location of a semiconductor IC comprising:
 - a [[means]] power supply for applying a power supply voltage to said semiconductor IC;
 - a [[means]] test pattern sequence input unit for supplying a test pattern sequence having a plurality of test patterns to said semiconductor IC;
 - a [[means]] <u>fault location list memory unit</u> for storing a fault location list for the test pattern sequence, wherein the fault location list includes one or more locations of

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components in said IC, and the electric potentials at the one or more locations are expected to change [[when]] <u>once</u> the test pattern sequence is supplied;

- a transient power supply current tester for measuring a time integral of a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern and determining whether said transient current shows abnormality or not; and
- a fault location presuming unit for presuming a fault location out of said fault location list, based on said test pattern sequence, where the transient power supply current shows abnormality, and said fault location list,
- wherein said transient power supply current tester determines that said transient power supply current is abnormal in <u>a</u> case <u>that the</u> time integral of said transient power supply current is over a predetermined value.

17 - 26. (Canceled)

- 27. (Currently Amended) A fault analysis apparatus for presuming configured to presume a fault location of <u>a</u> semiconductor IC comprising:
 - a [[means]] power supply for applying a power supply voltage to said semiconductor IC;
 - a [[means]] test pattern sequence input unit for supplying a test pattern sequence comprising a plurality of test patterns to said semiconductor IC;
 - a [[means]] <u>fault location list memory unit</u> for storing a fault location list for the test pattern sequence, wherein the fault location list includes one or more locations of components in said IC, and the electric potentials at the one or more locations are expected to change [[when]] <u>once</u> the test pattern sequence is supplied;
 - a means an integral transient power supply current measuring unit for measuring a time integral of a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern;
 - a [[means]] <u>fault detector</u> for determining that said transient <u>power supply</u> current is abnormal in <u>a</u> case <u>that the</u> time integral of said transient power supply current is over a predetermined value; and

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a [[means]] <u>fault location presuming unit</u> for presuming a fault location out of said location list, based on said test pattern sequence, where the transient power supply current shows abnormality, and said fault location list.